EXHIBIT H

DANIEL JOHNSON, JR. (State Bar No. 57409)
BRETT M. SCHUMAN (State Bar No. 189247)
MORGAN, LEWIS & BOCKIUS LLP
One Market, Spear Street Tower
San Francisco, CA 94105-1126
Tel: 415.442.1000
Fax: 415.442.1001
djjohnson@morganlewis.com
bschuman@morganlewis.com

ANDREW J. WU (State Bar No. 214442)
DAVID V. SANKER (State Bar No. 251260)
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, CA 94306-2122
Tel: 650.843.4000
Fax: 650.843.4001
awu@morganlewis.com
dsanker@morganlewis.com

Attorneys for Plaintiffs and Counterdefendants
ALPHA & OMEGA SEMICONDUCTOR, LTD.
ALPHA & OMEGA SEMICONDUCTOR, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

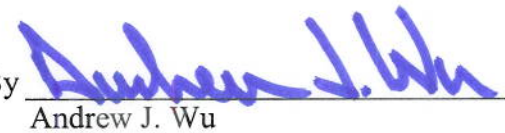
AOS'S PRELIMINARY CLAIM CONSTRUCTION PURSUANT TO PATENT LOCAL RULE 4-2

In accordance with Patent L.R. 4-2, Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, LTD and Alpha & Omega Semiconductor, Inc. ("AOS") submit this preliminary claim construction statement. Discovery in this case is still in the early stages and AOS's discovery and investigation in connection with this lawsuit are continuing. AOS believes that further extrinsic evidence, including expert or fact testimony, may assist in explaining the asserted claims and terms contained therein in view of claim interpretations advanced by Fairchild Semiconductor Corporation ("Fairchild"), the technical nature of the subject matter, the large number of patents and claims asserted, or a combination of these reasons.

Accordingly, AOS's preliminary claim construction, attached as Exhibit A, is given without prejudice to AOS's right to amend or supplement its disclosure after considering information obtained or reviewed through further discovery or investigation, or through the meet and confer process as outlined in the Patent Local Rules. Further, the consolidated list of proposed claim terms currently includes 37 terms, including 26 proposed by Fairchild. This greatly exceeds the ten-term limit imposed by the court's Standing Order for Patent Cases. AOS thus reserves the right to amend or supplement its disclosure as the list is reduced to ten terms.[1]

Dated: January 9, 2008

MORGAN, LEWIS & BOCKIUS LLP

By 
Andrew J. Wu

Attorneys for Plaintiffs and Counterdefendants ALPHA & OMEGA SEMICONDUCTOR, LTD. AND ALPHA & OMEGA SEMICONDUCTOR, INC.

[1] The parties may seek leave of the court to construe more than ten terms.

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

Term	Preliminary Construction
1. gate runners ('567, claim 7)	conductive gate stripes that divide the source contact area into several sub-contact areas; the stripes need not be contiguous
2. determining a total number of lead wires ('567, claim 7)	selecting the total number of lead wires to be connected to the source contact area
3. MOSFET power device('567, claim 7)	a semiconductor device used for power management, which is built using metal oxide semiconductor field-effect transistor (MOSFET) technology.
4. configuring said gate runners ('567, claim 7)	selecting a placement of gate runners on the source contact area and forming the gate runners according to that placement
5. several sub-contact areas ('567, claim 7)	two or more subdivisions of the source contact area
6. set of area proportional ratios ('567, claim 7)	the ratios of the areas of the sub-contact areas
7. several ('567, claim 7)	more than one
8. configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios ('567, claim 7)	the placement of gate runners divides the source contact area into sub-contact areas, and a set of area proportional ratios are defined by the ratios of the approximate areas of the sub-contact areas
9. disposing several of said lead wires in each of said sub-contact areas according to said set of area proportional ratios ('567, claim 7)	connecting two or more lead wires to each sub-contact area so that the ratio of lead wires to area is the same for each of the sub contact areas
10. compensating a portion of said body region by implanting material of said second conductivity type in said body region ('776, claims 1, 13, 25)	implanting into the body region material having conductivity type opposite the conductivity type of the body region
11. proximal to said source region ('776, claim 1)	near the source region
12. adjacent to said source region ('776, claims 13, 25)	near the source region
13. so as to reduce the impurity concentration of said first conductivity type in said portion of said body region ('776, claim 1)	to create a net reduction in impurity charge in the portion
14. substantially reduced so as to decrease the gate threshold voltage of said trench gate substantially reduced so as to	the impurity charge is reduced by a sizeable amount.

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

decrease the gate threshold voltage of said gate ('776, claims 13, 25)	
15. spaced from said diffusion boundary ('776, claims 1, 13, 25)	not touching the boundary between the body region and the substrate
16. applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates ('630, claim 1)	the meaning of this phrase is clear and unambiguous to a person of skill in the art, and thus it need not be construed by the court
17. overlying insulation layer ('630, claim 1)	a layer comprising an insulating material that is formed above the other layers
18. self-aligned ('630, claim 1)	the implant is performed without any additional mask applied to the region
19. top portion of said substrate ('630, claim 3)	a portion from the top of the substrate, which does not extend to the bottom of the source region
for etching said active layer ('630, claim 1)	for etching said <u>oxide</u> layer (typographical error in claim)
20. a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type a pair of doped source regions formed on opposite sides of the trench ('481, claims 1, 6, 15)	Fairchild no longer proposes to construe this term.
21. a doped well … formed into the substrate to a depth that is less than the predetermined depth of the trench a doped well … formed into the substrate to a second depth that is	the maximum depth of the doped well is less than the maximum depth of the trench

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

less than said first depth of the trench a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches a well between adjacent trenches to a second depth that is shallower than the first depth a plurality of doped wells … respectively to a second depth that is less than said first depth of the plurality of trenches ('481, claim 1; '406, claim 1; '195, claim 1; '111, claim 29)	
22. said heavy body extending into said doped well to a depth that is less than said depth of said doped well ('481, claim 1)	Fairchild no longer proposes to construe this term.
23. the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches the doped heavy body extending into the doped well to a second depth that is less than the first depth ('481, claims 6, 15)	Fairchild no longer proposes to construe this term.
24. wherein the heavy body forms an abrupt junction with the well wherein the doped heavy body … forms an abrupt junction with the well ('481, claims 1, 6, 15; '406, claims 1, 4, 5, 13; '195, claims 1, 21, 22)	the doping concentration gradient at the junction between the heavy body and the well is sufficiently high that the breakdown voltage at the p-n junction between the well and the substrate cannot be reduced any further by increasing the doping concentration gradient
25. depth of the junction, relative to the depth of the well, is adjusted so	selecting by repeated experiments or by computer simulation the relative depths of the well and the junction

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

that a transistor breakdown initiation point is spaced away from the trench in the semiconductor when voltage is applied to the transistor a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor ('481, claims 1, 6, 15; '406, claims 1, 13)	so that initiation of breakdown in the device is moved toward the center of the body region between adjacent trenches
26. patterning ('497, claims 1, 7)	Fairchild no longer proposes to construe this term.
27. wherein said dosage of said second dopant has a doping concentration that is greater than said dosage of said third dopant ('497, claim 1)	the dosage of the second dopant during implantation is greater than the dosage of the third dopant during implantation
28. double implant process ('195, claims 8, 9)	an implant is determined by dopant, dosage, and energy level; a double implant involves two implants, i.e., a first implant and a second implant, wherein at least one of dopant, dosage, or energy level of the second implant is different from that of the first implant
29. plurality of doped wells ('111,	Fairchild no longer proposes to construe this term.

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

claim 29)	
30. plurality of doped wells in the plurality of epitaxial mesas ('111, claim 29)	two or more doped wells are formed, each doped well must be formed in a region between two trenches
31. resulting in avalanche current that is substantially uniformly distributed ('111, claim 29)	the avalanche current at breakdown initiation is roughly equally distributed across the entire device
32. adjusting a dopant profile of the plurality of heavy body regions so that peak electric field is moved away from a nearby trench toward the heavy body ('111, claim 29)	selecting by repeated experiments or by computer simulation the relative depths of the well and the junction and the doping concentration gradient between the heavy body and the well so that the peak electric field is moved toward the centers of the cells, which are approximately halfway between adjacent trenches
33. epitaxial mesas ('111, claim 29)	the remaining flat-topped portion of the epitaxial layer after trenches have been formed in the epitaxial layer
34. acting as a field plate to extend the device breakdown voltage in the termination region ('947, claims 1, 5, 6)	forming a trenched conductive ring in the termination region, resulting in a higher breakdown voltage in the termination region by modifying the electric field distribution and causing modification of the depletion layer in the substrate
35. isolation trench ('947, claim 1)	a valley filled with dielectric material surrounded by sidewalls in the periphery of a semiconductor substrate that can prevent leakage into the substrate
36. a plurality of elongated inner runners extending in the same direction ('947, claim 6)	multiple substantially parallel gate trenches filled with a conductive material extending in one direction cross the active transistor region
37. single conductor ('947, claim 1)	a first conductor portion electrically coupled to a second conductor portion.
termination region ('947, claim 1)	a peripheral diffusion region with conductivity type the same as the body regions on the die surface that is not part of the active cell array

Exhibit A
AOS's Preliminary Claim Construction Pursuant to L.R. 4-2

I. PRELIMINARY DESIGNATION OF EXTRINSIC EVIDENCE UNDER 4-2(b)

AOS hereby designates the following evidence under Patent Local Rule 4-2(b), without admission that this constitutes "extrinsic evidence" as defined by the Federal Circuit or other relevant legal authority. AOS reserves the right to amend or supplement this list after receiving Fairchild's Patent L.R. 4-2 disclosure and the associated meet and confer communications.

Testimony: AOS anticipates that it may rely upon the testimony of an expert as to the understanding of the claim terms by someone of ordinary skill in the art. AOS may also rely upon the testimony of the inventors, prosecuting attorneys, or corporate representatives.

1. Oxford English Dictionary (online): definitions of adjacent, proximal, and several.

2. Pages 14, 728, 941, and 1073 of MERRIAM WEBSTER'S COLLEGIATE DICTIONARY (10th ed. 1997) (definitions of adjacent, mesa, proximal, and several).

3. Pages 16, 1167, and 1324 of MICROSOFT ENCARTA COLLEGE DICTIONARY (2001) (definitions of adjacent, proximal, and several).

4. S. M. Sze, PHYSICS OF SEMICONDUCTOR DEVICES (1981). FAIR0017267-FAIR0017314.

5. http://en.wikipedia.org/wiki/Finite_element_analysis

6. U.S. Patent No. 5,233,215.

DANIEL JOHNSON, JR. (State Bar No. 57409)
BRETT M. SCHUMAN State Bar No. 189247)
AMY M. SPICER (State Bar No. 188399)
MORGAN, LEWIS & BOCKIUS LLP
One Market, Spear Street Tower
San Francisco, CA 94105-1126
Tel: 415.442.1000
Fax: 415.442.1001
djjohnson@morganlewis.com
bschuman@morganlewis.com
aspicer@morganlewis.com

ANDREW J. WU (State Bar No. 214442)
DAVID V. SANKER (State Bar No. 251260)
MORGAN, LEWIS & BOCKIUS LLP
2 Palo Alto Square
3000 El Camino Real, Suite 700
Palo Alto, CA 94306-2122
Tel: 650.843.4000
Fax: 650.843.4001
awu@morganlewis.com
dsanker@morganlewis.com

Attorneys for Plaintiffs and Counterdefendants
ALPHA & OMEGA SEMICONDUCTOR, LTD.
ALPHA & OMEGA SEMICONDUCTOR, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-02638 JSW
(Consolidated with Case No. C-07-02664 JSW)

PROOF OF SERVICE

PROOF OF SERVICE

Alpha & Omega Semiconductor v. Fairchild Semiconductor

USND-C07-02638 JSW (Consolidated with C-07-02664 JSW)

I am a resident of the State of California and over the age of eighteen years, and not a party to the within action; my business address is 2 Palo Alto Square, 3000 El Camino Real, Suite 700, Palo Alto, CA 94306.

On **January 9, 2008**, I served the following document on the parties listed below:

- **AOS'S PRELIMINARY CLAIM CONSTRUCTION PURSUANT TO PATENT LOCAL RULE 4-2**
- **EXHIBIT A TO AOS'S PRELIMINARY CLAIM CONSTRUCTION PURSUANT TO PATENT LOCAL RULE 4-2**

☒	I caused the envelope(s) with the document(s) listed above to be **delivered by U.S. Mail**, to the addressee(s) noted below.

Addressee	**Service**
Eric Jacobs Igor Shoiket Matthew Hulse Leonard Augustine Priya Sreenivasan **TOWNSEND & TOWNSEND** 2 Embarcadero Center, 8th Floor San Francisco, CA 94111 Tel: 415.576.0200 **Fax: 415.576.0300**	**U.S. Mail**

I am readily familiar with the firm's practice of collection and processing correspondence for mailing. Under that practice it would be deposited with the U.S. Postal Service on that same day with postage thereon fully prepaid in the ordinary course of business. I am aware that on motion of the party served, service is presumed invalid if postal cancellation date or postage meter date is more than one day after date of deposit for mailing in affidavit.

Executed on **January 9, 2008**, at Palo Alto, California.

I declare under penalty of perjury, under the laws of the State of California, that the above is true and correct.

David V. Sanker